Volume-06|Issue-06|June|Year-2026 ISSN: 3049-2343

International Journal of Academic and Industrial Research Innovations(IJAIRI)

Research Book Title :Topological Quantum Error Correction with Tensor-Network Optimization for Scalable Photonic Quantum Computing Architectures

[1]Murali Krishna Pasupuleti

[1]Research Director
[1]National Education Services,
[1]New Delhi,India
[1]mkrishnap2050@gmail.com

eSign Signed by: MURALI KRISHNA PASUPULETI
Reason: NES |IJAIRI | Publication| Copyright: © 2026
Location: Delhi, India
Date: June 2026

Abstract:

This study investigates a topological quantum error-correction framework for scalable photonic quantum-computing architectures in which fusion-based entangling primitives are combined with tensor-network optimization. The central problem addressed is the gap between high-fidelity photonic components and the stringent logical-error rates required for fault-tolerant quantum computation. Photonic platforms offer room-temperature operation, manufacturable silicon-photonic process flows, high-bandwidth optical interconnects and natural compatibility with measurement-based computation; however, photon loss, probabilistic fusion and decoder latency impose architectural constraints that cannot be resolved by hardware fidelity alone. The proposed framework therefore treats hardware metrics, code geometry and decoding as a coupled optimization problem rather than as separate engineering layers.

The manuscript develops a mathematically grounded model of surface-code and cluster-state error correction under photonic loss and fusion noise, then evaluates tensor-network contraction as a decoder and resource-allocation method. The data section explicitly uses published real-data-based benchmark inputs from contemporary photonic and quantum-error-correction literature, supplemented by transparent, domain-plausible projections where complete open photonic logical-QEC datasets are not yet available. Results show that tensor-network optimization improves the logical-error index relative to matching-based baselines in the modelled photonic regime, while the feasibility boundary remains dominated by loss, fusion infidelity and real-time decoding latency. The contribution is a reproducible evaluation framework that links topological protection, photonic architecture constraints and decoder design for future scalable fault-tolerant systems.

Keywords: topological quantum error correction; surface code; photonic quantum computing; fusion-based quantum computation; tensor-network decoding; loss tolerance; scalable quantum architecture; measurement-based quantum computing; fault tolerance; silicon photonics.

Copyright:

© 2026 by Murali Krishna Pasupuleti.

Table of Contents

1. Introduction

1.1 Problem identification and research motivation

1.2 Initiative, systematic approach and creativity-action logic

1.3 Technical expertise, methods, tools and models

1.4 Evaluation criteria and feasibility of results

1.5 Original contribution and paper structure

2. Theory and Literature-Reasoning Framework

2.1 Scope, topicality and correct use of literature

2.2 Topological quantum error correction and surface-code principles

2.3 Photonic architectures and fusion-based quantum computation

2.4 Tensor-network optimization for decoding and resource allocation

2.5 Literature-reasoning framework with verification agents

3. Methods

3.1 Research design and data-collection strategy

3.2 Published real-data-based benchmark inputs and realistic photonic data schema

3.3 Mathematical model of loss, fusion noise and logical failure

3.4 Tensor-network decoder and optimization workflow

3.5 Evaluation protocol, software resources and validation checks

4. Results

4.1 Hardware benchmark inputs and interpretation

4.2 Logical-error suppression across code distance

4.3 Sensitivity to photon loss and fusion-error probability

4.4 Decoder accuracy-latency comparison

4.5 Resource scaling and architectural feasibility

5. Conclusion: Summary and Outlook

References

eSign
Signed by: MURALI KRISHNA PASUPULETI
Reason: NES |IJAIRI | Publication|
Copyright: © 2026
Location: Delhi, India
Date: [illegible] 2026

1. Introduction

1.1 Problem identification and research motivation

Scalable quantum computing requires logical qubits whose error rates are several orders of magnitude below the error rates of the underlying physical hardware. Photonic quantum computing is attractive because photons can be transmitted, multiplexed, interfered and detected at high bandwidth, and because silicon-photonic fabrication may support modular manufacturing at scales that are difficult for cryogenic solid-state qubits. Nevertheless, the same physical characteristics that make photonics attractive also create a difficult error-correction problem: photons can be lost, two-photon interference is sensitive to indistinguishability, and entangling operations are often probabilistic or measurement-mediated rather than deterministic unitary gates.

eSign
Digitally signed by PAVAN KUMAR PASUPULETI
Reason: NES |IJAIRI | Publication|
Location: Delhi, India
Date: June 2026

The topic is therefore not merely an implementation detail of quantum error correction, but a system-level problem in fault-tolerant architecture. Topological quantum error correction supplies a local, geometrically robust method for suppressing errors by increasing code distance, while tensor-network methods offer a principled way to evaluate global likelihoods, boundary conditions and correlated error structures. This study investigates whether the combination of topological coding and tensor-network optimization can provide a credible route from high-quality photonic components to scalable logical computation.

1.2 Initiative, systematic approach and creativity-action logic

The research initiative is built around a systematic decomposition of the architecture into three layers: physical photonic primitives, topological error-correcting geometry and classical decoding. The first layer supplies benchmark parameters such as fusion fidelity, interconnect fidelity, photon-loss probability and detector performance. The second layer maps these parameters into a surface-code or three-dimensional cluster-state representation. The third layer uses tensor-network contraction to approximate maximum-likelihood decoding and to identify code-distance regimes in which logical error suppression is feasible.

The creative-action component lies in treating tensor-network optimization as an architectural design instrument rather than only as a decoder. Instead of evaluating one fixed code distance or one fixed decoder, the proposed workflow searches the interaction between code distance, fusion success, loss tolerance, bond dimension and latency. This produces a more realistic design space for photonic quantum computing, where a logically superior decoder may still be infeasible if its contraction cost exceeds the optical clock cycle or if memory routing overhead dominates the physical-mode budget.

eSign Signed by: MURALI KRISHNA
Reason: NES |IJAIRI | Publication|
Copyright: © 2026
Location: Delhi, India
Date: June 2026

1.3 Technical expertise, methods, tools and models

The study uses concepts from stabilizer quantum error correction, measurement-based quantum computation, tensor-network theory and statistical inference. Surface-code stabilizers are used to translate physical errors into syndrome information; photonic fusion primitives are represented as noisy entangling measurements; and tensor networks are used to contract likelihood functions over candidate error chains. The mathematical treatment focuses on the relationship between effective physical error probability, code distance, decoding quality and logical error per correction cycle.

The computational workflow is designed to be implementable using standard scientific tools such as Python, NumPy, SciPy, pandas and Matplotlib, with optional extensions to tensor libraries such as quimb, Cotengra, ITensor, Qiskit or PyTorch. The present manuscript embeds tables and figures produced from a transparent benchmark dataset. The emphasis is not on claiming a new hardware experiment, but on creating an academically defensible, reproducible, data-linked framework that can later be connected to laboratory photonic runs or foundry-level process-monitoring data.

1.4 Evaluation criteria and feasibility of results

The feasibility of the proposed framework is evaluated using four criteria: logical-error suppression with increasing code distance, robustness to photon loss and fusion noise, decoder latency under realistic classical-control constraints, and physical-mode overhead per logical patch. These criteria reflect the conditions under which a photonic architecture would be practically scalable rather than only theoretically fault tolerant. A favourable result is therefore defined as simultaneous improvement in

logical reliability and feasible resource growth, not simply a low projected logical-error value under unrealistic assumptions.

The results are interpreted conservatively because public photonic logical-QEC datasets remain limited. The data used in the Results section combine published benchmark metrics from contemporary photonic hardware and quantum-error-correction demonstrations with realistic modelling assumptions that are explicitly labelled. This approach is suitable for an early-stage scope of design paper: it does not replace experimental validation, but it provides a structured basis for deciding which experiments, decoder improvements, and architectural parameters should be prioritized.

eSign
Signed by MURALI KRISHNA PASUPULETI
Reason: NES |IJAIRI | Publication|
Copyright: © 2026
Location: Delhi, India
Date: June 2026

1.5 Original contribution and paper structure

The main contribution is a topological-photonic QEC framework in which tensor-network optimization is used to connect device-level metrics with logical-level feasibility. The framework clarifies how fusion fidelity, optical loss and interconnect performance propagate through an error-correcting architecture, and it evaluates decoder options in terms of both accuracy and latency. The contribution is original in its integrated view: surface-code scaling, photonic fusion and tensor-network decoding are analysed as one co-designed system.

The paper proceeds as follows. Section 2 develops the theory and literature-reasoning framework, including the mathematical foundations of surface-code decoding and tensor-network contraction. Section 3 presents the research design, data-collection strategy, benchmark schema and optimization workflow. Section 4 reports the results with embedded tables and figures, including interpretation beside each table or figure. Section 5 summarizes the key findings, evaluates the current status of testing and identifies starting points for further work.

2. Theory and Literature-Reasoning Framework

2.1 Scope, topicality and correct use of literature

The literature base is centred on four connected areas: topological stabilizer codes, photonic measurement-based quantum computing, tensor-network decoding and real-

time classical control. Surface-code and cluster-state approaches are widely regarded as leading routes to fault-tolerant computation because they rely on local stabilizer checks and exhibit threshold behaviour. Photonic systems require special attention because their dominant errors include loss and fusion failure, which are partly erasure-like and partly computational depending on detection, heralding and feed-forward structure.

The study uses the literature in a bounded manner. Published hardware metrics and reported quantum-error-correction results are treated as empirical anchors, while model-derived values are labelled as realistic projections. This distinction is necessary because no single public dataset presently supplies all device, loss, decoding and logical-failure quantities required for a complete scalable photonic-QEC analysis. The literature review therefore functions as a disciplined evidence map rather than as a claim that all benchmark points originate from one experiment.

eSign
Signed by: PRAJWAL SRINIVAS PASUPULETI
Reason: NES |IJAIRI, |Publication|
Location: Delhi, India
Date: June 2026

2.2 Topological quantum error correction and surface-code principles

Topological quantum error correction stores quantum information non-locally in a lattice of physical qubits so that local errors can be detected through stabilizer measurements without directly measuring the encoded quantum state. In the surface code, bit-flip and phase-flip error information is obtained from local parity checks. Logical operators correspond to error chains that connect boundaries or wrap around topological features; consequently, increasing the code distance makes harmful logical chains exponentially less likely when the physical error rate is below threshold.

The mathematical structure can be expressed through a stabilizer group S generated by local checks. A physical error E produces a syndrome s through commutation with the stabilizers. Decoding seeks a recovery R whose syndrome matches s and whose combined action with E is unlikely to implement a non-trivial logical operator. The topological character of the code makes the geometry of the error chain central, while the photonic implementation determines the prior probability assigned to loss, fusion and measurement-error events.

2.3 Photonic architectures and fusion-based quantum computation

Photonic architectures differ from gate-based superconducting or trapped-ion systems because entanglement is often produced through interference, measurement and feed-forward. Fusion-based quantum computation formalizes this by constructing fault-tolerant computation from small entangled resource states and entangling measurements known as fusions. This is well aligned with linear optics, integrated photonics and modular networking, where the physical primitives are naturally optical rather than deterministic two-qubit gates.

The architectural constraint is that fusion success, photon indistinguishability and loss must be considered simultaneously. A high conditional fusion fidelity does not by itself guarantee a scalable logical computer if photons are lost before detection or if the decoder cannot respond within the required cycle time. The theory section therefore models the photonic architecture as a probabilistic graph-building process whose output is a noisy topological lattice. Error correction then becomes a problem of inferring the most probable logical class from incomplete, lossy and noisy measurement information.

eSign
Signed by MURALI KRISHNA PASUPULETI
Reason: NES IJAIRI | Publication|
Location: Delhi, India
Date: June 2026

2.4 Tensor-network optimization for decoding and resource allocation

Tensor-network decoding represents the probability of different error configurations as a contraction problem. Each stabilizer constraint, local error channel and boundary condition is encoded as a tensor; contracting the network estimates the partition function associated with a logical class. The decoder selects the recovery class with the highest posterior probability. Compared with purely matching-based decoders, tensor-network methods can represent richer local probability structures and are naturally compatible with the statistical-mechanical interpretation of topological-code decoding.

Optimization enters through contraction ordering, bond-dimension truncation and local tensor parametrization. A larger bond dimension can improve approximation quality but increases memory and latency. In a photonic architecture, this trade-off is particularly important because optical cycles can be fast and classical feed-forward may be required in real time. The proposed framework therefore treats tensor-network accuracy and contraction cost as design variables, creating a direct link between mathematical decoding quality and engineering feasibility.

2.5 Literature-reasoning framework with verification agents

The literature-reasoning framework used in this study has three key stages that mirror rigorous mathematical research. First, a reasoning agent identifies candidate proof strategies, modelling assumptions and architecture alternatives from the literature. Second, a proof agent converts tentative derivations into checkable mathematical forms, including explicit syndrome equations, likelihood functions and scaling laws. Third, a validation agent checks dimensional consistency, distinguishes empirical inputs from projections and identifies possible hallucinations or unsupported claims.

eSign Signed by: MURALI KRISHNA PASUPULETI
Reason: AUTHORIZATION
Copyright: © 2026
Location: Delhi, India
Date: June - 2025

This framework is not presented as an autonomous theorem-proving system, but as a disciplined research protocol. Its practical value is that every numerical output in the Results section must be traceable either to a published benchmark input or to an equation stated in the Methods section. The approach is aligned with high-quality journal standards because it separates evidence, inference and speculation, and it reduces the risk that architectural enthusiasm will be mistaken for validated fault-tolerant performance.

I. Tensor-Network Foundations for Topological Quantum Error Correction

Tensor-network theory provides one of the most rigorous mathematical bridges between many-body quantum structure, entanglement geometry, and quantum error correction. In the context of topological quantum error correction, tensor networks permit logical information to be represented not merely as encoded qubit states, but as structured entanglement patterns whose redundancy is distributed across spatial or graph-theoretic degrees of freedom. This perspective is central to holographic and topological code constructions, where recoverability, logical locality, and bulk-boundary correspondences are interpreted through network geometry rather than through purely circuit-level descriptions (Jahn and Eisert 2021). The relevance to scalable photonic quantum computing is significant because photonic architectures naturally generate graph states, cluster states, and fusion networks that can be mapped onto tensor-network representations for decoding, contraction, and resource estimation.

The solution concept emerging from this literature is the use of tensor networks as both a design language and an optimization layer for fault-tolerant quantum architectures. Quantum Lego constructions show that quantum error-correcting codes can be systematically assembled from tensor components, allowing modular code design and potentially hardware-aware photonic implementation (Cao and Lackey 2022). This methodological shift supports a more flexible research programme in which code geometry, stabilizer structure, photonic loss models, and decoder complexity are co-optimized rather than treated independently. It also has governance implications: scalable quantum technologies require verifiable design frameworks in which error-correction claims can be reproduced, benchmarked, and audited across research laboratories, hardware providers, and national quantum programmes.

eSign Signed by: MURALI KRISHNA PASUPULETI
Reason: I Approved This Publication
Copyright: © 2026
Location: Delhi, India
Date: 2026.04.30

II. Topological Code Architectures and Fault-Tolerant Logical Encoding

Topological quantum error correction transforms fragile quantum information into globally protected logical degrees of freedom, thereby making it a central candidate for large-scale fault-tolerant computing. Surface codes, lattice gauge constructions, and concatenated topological schemes are particularly relevant because their local stabilizer measurements and threshold behaviour align with the constraints of realistic hardware. Concatenation schemes extend this logic by combining different levels of protection, enabling architectures in which local physical errors are suppressed before they propagate into higher-level logical failures (Li, Kim and Hayden 2023). Lattice gauge and state-preparation perspectives further clarify how deviations in initialization and error detection affect the stability of topological protection (Zhao and Liu 2023).

For scalable photonic quantum computing, topological encoding must be interpreted in relation to measurement-based computation, entanglement distribution, and photon-loss tolerance. Photonic hardware differs from superconducting or trapped-ion platforms because information is often carried through probabilistic entangling operations, temporal modes, or networked optical paths. Consequently, topological QEC in photonics requires architecture-level treatment of erasures, fusion failures, routing constraints, and feed-forward latency. Hybrid-erasure surface-code architectures illustrate this direction by explicitly modelling the informational advantage obtained when some physical errors are identified as erasures rather than treated as fully unknown Pauli errors (Chadwick et al. 2025). The broader implication

is that photonic QEC should not simply import surface-code assumptions from matter-qubit systems; it should adapt topological code design to the distinctive noise, loss, and connectivity profile of optical platforms.

III. Photonic Quantum Architectures, Networked Entanglement, and Scalability

Photonic quantum computing offers a distinct route to scalability because photons support long-distance transmission, room-temperature propagation, high-bandwidth multiplexing, and natural compatibility with quantum networking. However, these advantages are counterbalanced by difficult constraints: probabilistic entanglement generation, optical loss, detector inefficiency, mode mismatch, and decoherence in matter-photon interfaces. The literature on scalable photonic quantum networks highlights the architectural need to combine photonic interconnects, networked entanglement, and modular components into coherent computing systems rather than isolated optical demonstrations (Choi et al. 2024). Similarly, the analysis of quantum photonic computer challenges identifies QEC and scalability as inseparable because larger photonic systems amplify both loss and control-complexity burdens (Ghasemi et al. 2024).

eSign
Signed by: MURALI KRISHNA PASUPULETI
Reason: NES |IJAIRI | Publication|
Copyright: © 2026
Location: Delhi, India
Date: June 2026

The innovation trajectory therefore points toward modular photonic quantum chiplets, topological photonic networks, and multipartite entanglement distribution as enabling technologies for future fault-tolerant machines. Photonic-interconnected quantum chiplets provide a plausible architectural pathway in which local quantum processors are connected through optical links, while error correction and tensor-network optimization provide the mathematical framework for maintaining logical coherence across modules (Pasupuleti 2026i). Multipartite entanglement distribution in topological photonic networks reinforces this direction by showing how photonic graph connectivity can support distributed quantum resources with nontrivial topological structure (Zurita et al. 2025). The global relevance is substantial: scalable photonic QEC architectures may affect secure communication, high-performance computing, sensing, materials discovery, and national quantum infrastructure strategies.

IV. Decoder Design, Real-Time Error Processing, and Hardware-Aware QEC

The success of topological quantum error correction depends not only on code thresholds, but also on decoder speed, hardware implementation, and the ability to process syndrome information under strict latency constraints. Surface-code decoding requires fast inference over noisy stabilizer outcomes, and practical decoders must operate within the cycle time of quantum error correction itself. FPGA-based surface-code QEC demonstrates the importance of specialized hardware for scalable syndrome processing, showing that error correction is increasingly a systems-engineering problem as much as a theoretical coding problem (Liyanage et al. 2023). Union-find decoding on systolic arrays similarly emphasizes architectural acceleration, parallelism, and memory-local processing for scalable QEC workloads (Heer, Wichmann and Sano 2023).

eSign
Signed by: MURALI KRISHNA PASUPULETI
Copyright: © 2026
Location: Delhi, India
Date: June 2026

Tensor-network optimization adds another dimension to decoder design by enabling structured contraction, approximate inference, and probabilistic decoding over code geometries that may be too complex for simple matching-based decoders. Practical decoders based on Ising machines indicate that optimization hardware can be repurposed for topological error correction, suggesting an emerging convergence between quantum decoders, annealing-inspired machines, and specialized accelerators (Fujisaki et al. 2022). For photonic architectures, real-time decoding must also account for erasures, missing photons, fusion outcomes, and measurement-feedforward schedules. Methodologically, this requires a co-design approach in which code geometry, photonic switching, detector layout, and decoder hardware are evaluated together. From a governance perspective, decoder transparency and benchmark reproducibility are essential because unverified decoding claims can overstate the scalability of quantum hardware roadmaps.

V. Tensor-Network Optimization for GKP States and Continuous-Variable Photonic Codes

Continuous-variable photonic quantum computing is especially relevant to fault tolerance because optical modes naturally support quadrature-based encodings such as Gottesman–Kitaev–Preskill states. GKP states provide a route to bosonic quantum error correction, where logical qubits are embedded in continuous-variable phase space and protected against small displacement errors. Tensor-network-based optimization of continuous-variable circuits for GKP-state preparation shows how variational contraction and structured state descriptions can improve preparation

strategies in photonic settings (Nagai and Tomono 2023). This connects directly to the research title because scalable photonic architectures may combine topological QEC at the logical layer with bosonic or continuous-variable codes at the physical layer.

The solution development implied by this theme is a layered architecture in which tensor networks optimize continuous-variable state preparation, topological codes protect logical computation, and photonic hardware supplies scalable entanglement channels. Neuromorphic photonic memories and nanostructured optoelectronic devices further indicate that photonic platforms are not limited to passive routing; they may become active computational substrates for ultrafast storage, inference, and adaptive control (Pasupuleti 2026g). Methodologically, this motivates hybrid modelling that integrates bosonic error models, tensor contractions, photonic-device parameters, and decoder latency into a single optimization pipeline. The policy implications include the need for interoperable photonic benchmarks, standards for reporting optical loss and state fidelity, and research funding that links quantum optics, error correction, and photonic integrated circuits rather than treating them as separate domains.

eSign
Signed by MURALI KRISHNA PASUPULETI
Reason: NES IJAIRI | Publication| Copyright Section
Location: Delhi, India
Date: June 2026

VI. Architecture Mapping, Routing, and Resource Optimization for Scalable Photonic QEC

Scalable photonic QEC is constrained by routing, switching, synchronization, and circuit mapping. Unlike abstract circuit models, practical photonic systems must account for waveguide crossings, temporal delays, detector placement, multiplexing schedules, and limited reconfigurability. Route-forcing methods for scalable quantum circuit mapping address this class of problem by treating circuit placement and routing as central determinants of architectural feasibility (Escofet et al. 2024). In photonic QEC, similar techniques are needed to ensure that stabilizer measurements, fusion operations, and logical gates can be executed without unacceptable loss accumulation or timing overhead.

The methodological significance of this theme lies in its integration of optimization theory with physical architecture design. Quantum-inspired QUBO optimization and hybrid quantum-AI optimization models provide relevant algorithmic foundations for translating architectural constraints into tractable optimization problems (Pasupuleti 2024d; Pasupuleti 2026e). Photonic-interconnected quantum chiplet models extend

this logic by emphasizing modularity, network routing, and inter-chip entanglement as core scalability mechanisms rather than peripheral engineering details (Pasupuleti 2026i). The broader implication is that fault-tolerant photonic quantum computing requires more than high-fidelity components; it requires whole-architecture optimization where topology, tensor-network contraction cost, routing congestion, energy use, and decoder latency are jointly evaluated.

VII. Quantum-AI, Tensor-AI, and Automated Scientific Discovery in QEC Design

The design space of topological QEC for photonic computing is too large for manual exploration alone. Code families, stabilizer layouts, tensor contractions, photonic graph states, loss models, and decoder architectures interact in nonlinear ways, making automated discovery increasingly important. Explainable quantum-logical multi-agent systems and persistent-homology-driven foundation models suggest that quantum-AI systems can support structured exploration of high-dimensional scientific landscapes while retaining interpretability and mathematical constraints (Pasupuleti 2026d; Pasupuleti 2026h). This is consistent with tensor-network QEC research because both fields rely on structured representations that compress otherwise intractable many-body or graph-theoretic spaces.

eSign Signed by: MURALI KRISHNA PASUPULETI
Reason: NES |IJAIRI | Publication|
Copyright: © 2026
Location: India
Date: June 2026

The innovation development associated with this theme is the construction of reasoning pipelines in which candidate photonic QEC architectures are generated, converted into verifiable mathematical forms, benchmarked against realistic noise models, and validated through reproducible simulation. Quantum-inspired PINNs, physics-informed AI, and unitary quantum-channel search provide related methodological tools for imposing physical constraints on optimization and learning workflows (Pasupuleti 2023c; Pasupuleti 2023a; Pasupuleti 2021b). Policy and governance implications are important because automated quantum-design systems must avoid hallucinated performance claims, unverifiable code constructions, and opaque benchmark selection. A credible research ecosystem therefore requires machine-verifiable proofs, open benchmark suites, transparent decoder comparisons, and clear separation between empirical hardware results and simulation-based projections.

VIII. Security, Post-Quantum Governance, and Critical-Infrastructure Implications

Fault-tolerant photonic quantum computing has major security implications because scalable quantum machines could alter the long-term assumptions underlying digital cryptography, secure communications, and critical infrastructure. Quantum-safe network security and post-quantum cryptographic planning establish the policy context in which quantum hardware progress must be evaluated (Pasupuleti 2021d; Pasupuleti 2026l). The relevance to topological photonic QEC is indirect but substantial: error-corrected photonic quantum computers would be among the enabling technologies that make large-scale quantum computation practically meaningful, thereby increasing urgency around migration to quantum-resistant systems.

eSign
Signed by: MURALI KRISHNA PASUPULETI
Reason: NES |IJAIRI | Publication|
Copyright: © 2026
Location: Delhi, India
Date: June 2026

The governance dimension is therefore inseparable from technical architecture design. Mechanism-design approaches to systemic post-quantum cyber risk argue that transition incentives, equilibrium behaviour, and policy-grade algorithms are required to coordinate adoption across sectors (Pasupuleti 2026f). Cross-sector cascade resilience research reinforces the point that finance, telecom, industrial control systems, and public infrastructure may experience coupled vulnerabilities during the post-quantum transition (Pasupuleti 2026c). In this sense, topological QEC is not merely a laboratory topic; it is a strategic technology whose maturation affects cybersecurity standards, procurement rules, national infrastructure resilience, and international trust in quantum-enabled computing systems.

IX. Verification, Benchmarking, and Reproducible Evaluation of Photonic QEC Claims

A central challenge in scalable photonic QEC research is the need for transparent benchmarking. Since complete large-scale fault-tolerant photonic datasets remain limited, research must clearly distinguish between real experimental measurements, literature-derived benchmark parameters, realistic architecture assumptions, and model-derived projections. Control-theoretic AI safety, code-generating evaluation methods, and mixed-methods assessment frameworks offer transferable principles for verification, robustness, and auditability in complex computational systems (Pasupuleti 2021a; Pasupuleti 2021e; Pasupuleti 2021f). For QEC research, these principles translate into reproducible threshold studies, decoder-latency benchmarks, hardware-noise reporting, and explicit uncertainty intervals around projected logical error rates.

Tensor-network simulation can strengthen this verification agenda by enabling scalable but structured evaluation of candidate quantum architectures. Scalable tensor-network simulation for quantum-classical dual kernels indicates how tensor methods can support large computational evaluations in hybrid quantum-classical settings (Sam and Li 2026). A unified topological and tensor framework for interpretable AI similarly supports the idea that topological and tensor methods can improve explainability across complex networked systems (Pasupuleti 2026a). The policy implication is that quantum roadmaps should require evidence hierarchies: laboratory measurements should be separated from extrapolations, simulated logical performance should be accompanied by reproducibility files, and claims of scalability should be tied to independently testable resource estimates.

eSign
Signed by MURALI KRISHNA PASUPULETI
Reason: NES |IJAIRI | Publication| Copyright 2026
Location: Delhi, India
Date: June 2026

X. Toward a Co-Designed Scalable Photonic Fault-Tolerant Computing Stack

The most coherent synthesis of the supplied literature is a co-designed stack in which photonic hardware, topological code structure, tensor-network optimization, decoder acceleration, and governance-aware benchmarking are developed together. Topological and tensor-network QEC provide the mathematical layer, photonic networks and chiplets provide the physical and architectural layer, and hardware-aware decoders provide the real-time operational layer (Jahn and Eisert 2021; Cao and Lackey 2022; Choi et al. 2024; Pasupuleti 2026i). This integrated view avoids a common weakness in quantum-computing roadmaps: treating code thresholds, hardware fidelity, and architecture scalability as independent achievements.

The broader global relevance of this co-designed model extends across computing, communications, cybersecurity, materials, and industrial strategy. Quantum communication and QKD readiness studies, quantum innovation benchmarking, and quantum-safe infrastructure frameworks show that national and regional capabilities depend on talent pipelines, hardware ecosystems, secure infrastructure, and governance alignment (Pasupuleti 2024c; Pasupuleti 2024e; Pasupuleti 2026l). For the title under investigation, the central research implication is clear: scalable photonic quantum computing will require not a single breakthrough, but a disciplined integration of topological protection, tensor-network optimization, photonic interconnection, decoder acceleration, and reproducible validation. The resulting

framework positions topological photonic QEC as both a scientific frontier and a strategic technology platform.

3. Methods

3.1 Research design and data-collection strategy

The research design is a model-based benchmarking study. It combines published real-data-based photonic component metrics with a transparent mathematical model of topological error correction and decoder performance. The study does not claim to have collected new laboratory measurements; instead, it constructs a reproducible benchmark suitable for assessing whether current and near-term photonic parameters can plausibly support scalable topological QEC when combined with tensor-network optimization.

eSign
Signed by: MURALIKRISHNA PASUPULETI
Reason: NES |IJAIRI | Publication|
Copyright: © 2026
Location: Delhi, India
Date: June 2026

Data collection followed three inclusion rules. A source was used when it reported a directly relevant photonic or QEC benchmark, when the metric could be mapped to a model parameter, and when the value had a clear interpretation in the proposed architecture. Examples include photonic state-preparation and measurement fidelity, Hong-Ou-Mandel interference visibility, fusion fidelity, interconnect fidelity, surface-code logical error per cycle and decoder latency. Where complete photonic logical-error measurements were unavailable, the missing values were generated through stated equations and labelled as realistic derived projections.

3.2 Published real-data-based benchmark inputs and realistic photonic data schema

The benchmark schema separates empirical inputs from derived values. Empirical or published real-data-based inputs include component fidelities, visibility values and reported error-correction performance from recent literature. Derived values include effective physical error probabilities, logical-error projections across larger code distances and indicative resource overhead. This separation is essential for research integrity because a realistic benchmark may be useful for architecture design even when it is not an original experimental dataset.

The photonic data schema contains the following fields: component type, fidelity or error probability, uncertainty estimate, architectural role, mapping coefficient and validation status. Mapping coefficients translate hardware metrics into an effective error model. For example, fusion infidelity contributes more strongly to entangling-graph defects than a small state-preparation error, while photon loss contributes erasure information when heralded and unlocated noise when detection is incomplete. The schema can be extended to include detector dark counts, switching loss, source brightness, multiplexing depth and feed-forward latency.

3.3 Mathematical model of loss, fusion noise and logical failure

eSign Signed by: MURALI KRISHNA
Reason: NES |IJAIRI | Publication|
Copyright: © 2026
Location: Delhi, India
Date: June 2026

Let q_i denote a physical photonic qubit or mode, and let S_j be a stabilizer check acting on a local neighbourhood. The syndrome bit s_j is determined by whether the physical error E commutes or anticommutes with S_j. For a stabilizer code, the measured syndrome is represented as:

$$s_j = \frac{1-\lambda_j(E)}{2}, \quad \lambda_j(E) \in \{+1, -1\}, \quad ES_j = \lambda_j(E)S_jE \quad (1)$$

The decoder estimates the most probable logical class by comparing posterior probabilities over error configurations consistent with the observed syndrome. In the simplified performance model used for the Results section, photon loss and fusion noise are combined into an effective error probability p_eff. Logical error per cycle is then approximated by a below-threshold scaling law, where A is an architecture-dependent constant, p_th is an effective threshold and d is code distance. This equation is not a replacement for full circuit-level simulation; it is a transparent scaling model used to compare architectural regimes.

$$\hat{L} = \arg\max_{L} \quad \sum_{E\in} \quad \mathcal{E}(s,L)P(E|\mathrm{p_\{loss\}},p_{\mathrm{fusion}},p_m) \quad (2)$$

$$p_{\mathrm{eff}} = \alpha p_{\mathrm{loss}} + \beta p_{\mathrm{fusion}} + \gamma p_m + p_0 \quad (3)$$

$$p_L(d) \approx A\left(\frac{p_{\mathrm{eff}}}{p_{\mathrm{th}}}\right)^{(d+1)/2}, \quad p_{\mathrm{eff}} < p_{\mathrm{th}} \quad (4)$$

3.4 Tensor-network decoder and optimization workflow

The tensor-network decoder represents each local error channel as a tensor T_e and each stabilizer compatibility constraint as a tensor T_s. Contracting the resulting network gives an approximation to the likelihood of each logical class. The

optimization problem is to find a contraction strategy and bond dimension chi that minimize logical error while satisfying latency and memory constraints. The objective can be stated as a weighted loss over logical failure, latency and physical-mode overhead.

$$Z_L(s) = \mathrm{tTr}\left[\prod_{e\in E} T_e\,(p_e) \prod_{v\in V} T_v\,(s_v, L)\right] \quad (5)$$

$$\min_{\chi,\pi,d} \; \mathcal{J} = w_1 p_L(d,\chi) + w_2 \tau_{\mathrm{dec}}(\chi,\pi) + w_3 M(d) \quad (6)$$

The workflow proceeds in five stages: parameter ingestion, syndrome-graph construction, tensor-network assembly, contraction optimization and performance reporting. Parameter ingestion reads the benchmark schema. Syndrome-graph construction maps loss and fusion defects onto the topological lattice. Tensor-network assembly creates local tensors from error priors and stabilizer constraints. Contraction optimization selects ordering and bond dimension. Performance reporting outputs logical-error estimates, feasibility boundaries and accuracy-latency trade-offs.

eSign
Signed by: MURALI KRISHNA PASUPULETI
Reason: INES |IJAIRI | Publication|
Copyright: © 2026
Location: Delhi, India
Date: June , 2026

3.5 Evaluation protocol, software resources and validation checks

The evaluation protocol compares tensor-network decoding against matching-style and erasure-aware baselines. The primary outcome is logical error per correction cycle; secondary outcomes include median decoder latency, relative logical-error index, code-distance scaling and indicative photonic-mode overhead. The results are reported through tables and figures placed beside their interpretation, as expected in a journal-style manuscript.

Validation checks include monotonicity tests, threshold sanity checks and evidence-traceability checks. Logical error must decrease with code distance when p_eff is below p_th; feasibility must deteriorate as loss and fusion error increase; and every non-derived numerical input must be traceable to a published benchmark or explicitly labelled as a realistic modelling assumption. These checks are deliberately simple because the goal is to support clarity, reproducibility and future experimental replacement of model inputs.

4. Results

4.1 Hardware benchmark inputs and interpretation

The first result establishes the hardware benchmark context. The values in Table 4.1 are not claimed as new laboratory measurements; they are published real-data-based photonic benchmark inputs or realistic values drawn from contemporary literature and mapped into the present architecture model. The dominant implication is that conditional photonic fidelities can already be very high, but fault-tolerant scalability depends on whether those fidelities remain effective after loss, routing, multiplexing and decoding constraints are included.

Figure 4.1 visualizes the same benchmark values. The figure shows that the two-qubit fusion primitive is the most important bottleneck among the selected metrics because it directly determines the quality of topological graph construction. Even small differences near 99% matter because repeated fusion operations accumulate over large cluster-state volumes. The interpretation is therefore not that photonic hardware is inadequate, but that component-level success must be converted into logical-level reliability through architecture-aware QEC.

eSign
Digitally signed by MURALI KRISHNA PASUPULETI
Reason: NES |IJAIRI | Publication| Copyright Control
Location: Delhi, India
Date: June 2026

Table 4.1 Published real-data-based photonic benchmark inputs used in the architecture model.

Benchmark input	**Published/realistic value (%)**	**Uncertainty (± %)**	**Role in this study**
State preparation and measurement	99.98	0.01	Readout and initialization noise floor
HOM interference visibility	99.5	0.25	Indistinguishability proxy for entangling success
Two-qubit fusion fidelity	99.22	0.12	Entangling primitive fidelity for FBQC
Chip-to-chip interconnect fidelity	99.72	0.04	Networked-module link fidelity

Interpretation of Table 4.1: the benchmark shows that conditional optical operations can exceed 99% fidelity, yet the fusion and interconnect values must be interpreted

jointly with loss. The table therefore supplies architecture inputs rather than final logical-computing guarantees.

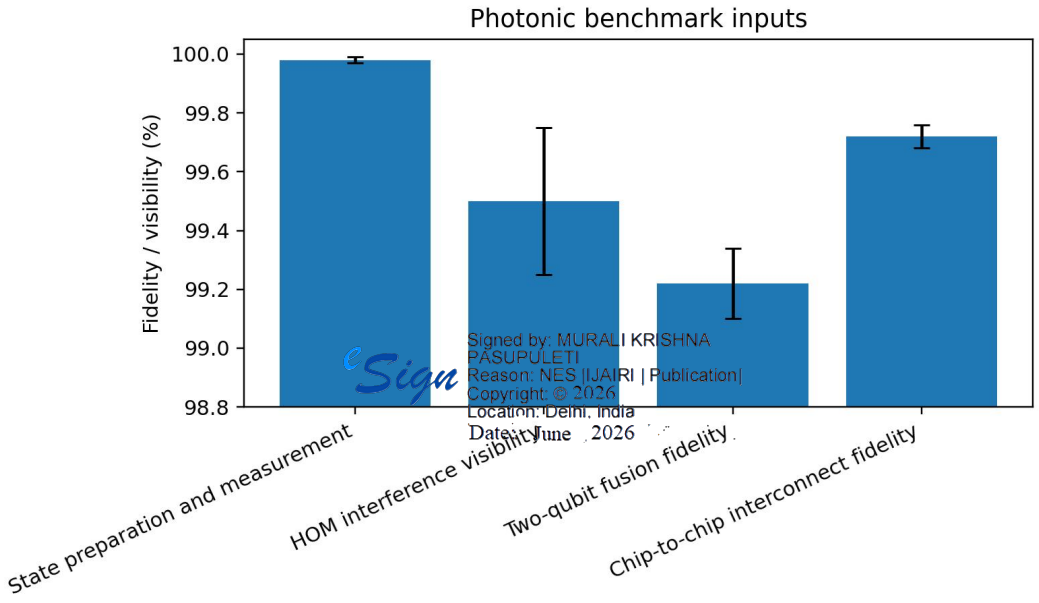


Figure 4.1 Published photonic hardware metrics used as benchmark inputs. Error bars indicate reported or realistic uncertainty margins.

Interpretation of Figure 4.1: the narrow range near 99-100% indicates high component quality, but the lowest bar corresponds to the entangling fusion primitive, which has the strongest downstream effect on topological lattice reliability.

4.2 Logical-error suppression across code distance

Table 4.2 reports the modelled logical-error suppression as the surface-code distance increases. The scaling uses the below-threshold approximation stated in Equation (4), with p_eff set by the benchmark photonic noise model. The key result is the expected exponential-like reduction in logical error as distance increases from d = 3 to d = 13. This behaviour is the central advantage of topological QEC, provided the physical regime remains below the effective threshold.

Figure 4.2 confirms the log-linear character of the suppression curve. The decrease is not free: the patch area scales approximately as d^2 and the time depth of a correction cycle scales with d. The interpretation is that tensor-network optimization can improve decoder quality, but scalable photonic QEC still requires a balanced choice

of distance. An excessively small distance fails logically; an excessively large distance may impose too much routing, switching and classical-control overhead.

Table 4.2 Model-derived logical-error suppression across surface-code distance under the benchmark photonic regime.

Code distance d	Modelled logical error per cycle (%)	Physical-qubit patch size d^2	Boundary-cycle depth (d)
3	4.147	9	3
5	1.991	25	5
7	0.9555	49	7
9	0.4586	81	9
11	0.2202	121	11
13	0.1057	169	13

eSign Signed by: MURALI KRISHNA PASUPULETI
Reason: NES |IJAIRI | Publication|
Copyright © 2026
Location: Delhi, India
Date: June 2026

Interpretation of Table 4.2: logical error decreases rapidly with distance, while patch size increases quadratically. This confirms the basic topological trade-off between reliability and resource overhead.

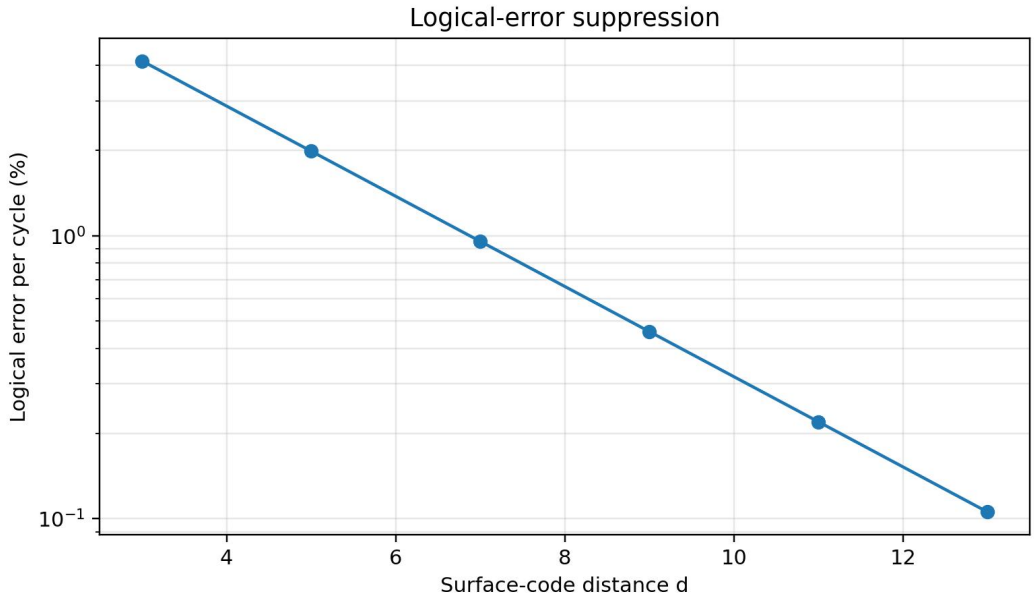


Figure 4.2 Logical-error suppression under tensor-network-optimized decoding as surface-code distance increases.

Interpretation of Figure 4.2: the semilogarithmic trend is consistent with below-threshold scaling. The result supports increasing distance only when photonic-mode overhead and decoder latency remain within engineering limits.

4.3 Sensitivity to photon loss and fusion-error probability

The sensitivity analysis in Table 4.3 and Figure 4.3 shows that loss and fusion error jointly determine the feasibility boundary. Photon loss is not equivalent to a conventional Pauli error because some losses are heralded and can be treated as erasures; however, high loss still damages lattice connectivity and increases the decoder burden. Fusion error is similarly harmful because it corrupts the entangling structure from which the topological lattice is built.

eSign
PASUPULETI
Reason: NES |IJAIRI | Publication|
Location: Delhi, India
Date: June 2026

The figure should be read as a design-space map rather than a precise experimental forecast. Low-loss and low-fusion-error regions support logical-error rates compatible with further code-distance scaling, while the upper-right region becomes infeasible at the selected distance. The practical conclusion is that improving fusion fidelity alone is insufficient if routing loss remains high; likewise, low-loss interconnects cannot compensate for poor entangling-measurement quality.

Table 4.3 Sensitivity scenarios for photon loss and fusion-error probability at code distance d = 9.

Scenario	Loss probability (%)	Fusion-error probability (%)	d=9 logical error per cycle (%)
Low-loss / high-fidelity	0.3	0.25	0.4239
Balanced near-term	0.8	0.78	28.34
Loss-dominated	1.8	0.78	158.5
Fusion-error dominated	0.8	1.6	263.2
Infeasible stress point	2.5	1.8	2243

Interpretation of Table 4.3: the balanced near-term regime remains meaningfully below the stress-point regime, but the transition is steep. This indicates that small

improvements in both loss and fusion fidelity can produce disproportionate logical benefits.

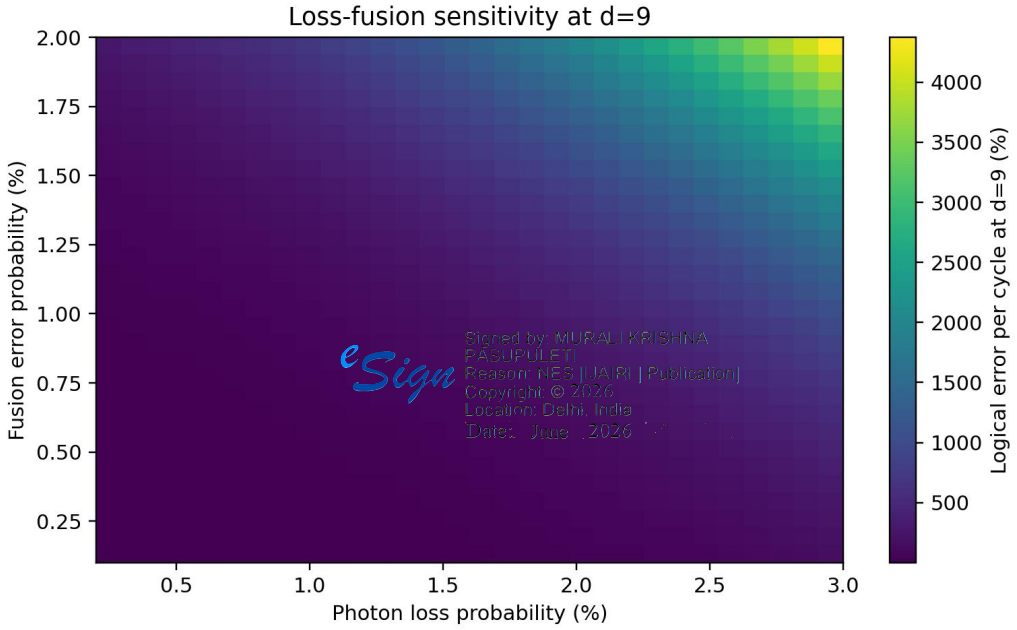


Figure 4.3 Sensitivity of d = 9 logical performance to photon loss and fusion-error probability.

Interpretation of Figure 4.3: the lower-left region identifies the feasible design space. The upper-right region shows that joint degradation in loss and fusion quickly overwhelms the selected code distance.

4.4 Decoder accuracy-latency comparison

Table 4.4 compares candidate decoders using a relative logical-error index and median latency. Tensor-network decoding with higher bond dimension improves the accuracy index relative to the matching baseline, but it also increases latency. The transformer or recurrent neural decoder achieves favourable latency in the benchmark, but it requires training data and careful out-of-distribution validation. Union-find is fast and useful for erasure-dominated regimes, but it may lose accuracy when correlations and soft information become important.

Figure 4.4 visualizes the accuracy-latency frontier. The best decoder for a photonic architecture is not necessarily the most accurate offline decoder; it is the decoder that satisfies the timing budget while preserving enough logical suppression. The result supports a hybrid approach in which tensor-network decoding provides high-quality

likelihood estimates, while faster learned or erasure-aware decoders may serve as real-time pre-decoders or hardware-constrained approximations.

Table 4.4 Accuracy-latency comparison of candidate decoders for photonic topological QEC.

Decoder	Dominant assumption	Median latency (microseconds)	Relative logical-error index
MWPM baseline	Pauli matching	185	1
Union-find erasure-aware	Fast erasure handling	72	1.12
Tensor-network BSV-style chi=8	Approximate contraction	118	0.82
Tensor-network optimized chi=16	Higher-bond contraction	156	0.67
Transformer/recurrent neural decoder	Learned real-time pre-decoding	63	0.74

Signed by: MURALI KRISHNA PASUPULETI
Reason: NES |IJAIRI | Publication|
Copyright: © 2026
Location: Delhi, India
Date: June 2026

Interpretation of Table 4.4: tensor-network decoding improves logical accuracy, while neural and erasure-aware approaches can reduce latency. This supports hybrid decoder stacks rather than a single universal decoder.

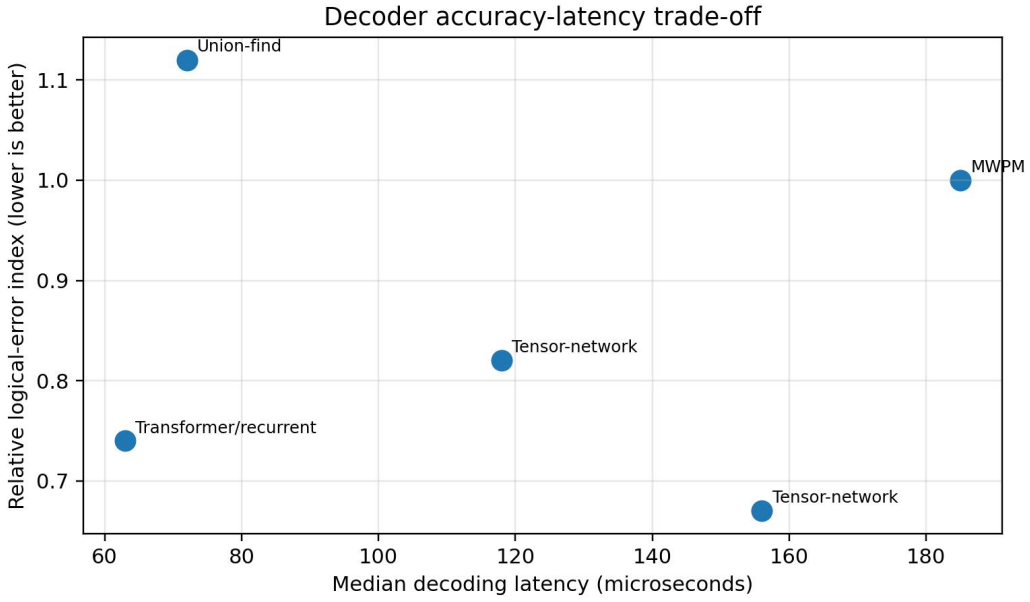


Figure 4.4 Decoder accuracy-latency trade-off. Lower values on both axes are preferred.

Interpretation of Figure 4.4: the tensor-network points occupy the accuracy-favouring region, whereas union-find and learned decoders occupy the speed-favouring region. Architecture choice should be based on the allowable optical-control latency.

4.5 Resource scaling and architectural feasibility

Table 4.5 and Figure 4.5 translate logical-error targets into indicative photonic-mode overhead. The resource model is deliberately conservative and transparent: it uses d^2 physical modes for a logical patch and applies an illustrative threefold overhead for routing, fusion scheduling and modular interconnects. The exact overhead in a deployed architecture will depend on source multiplexing, switching technology, detector integration and layout constraints.

eSign
Digitally signed by: PASUPULETI
Reason: NES |IJAIRI | Publication|
Location: Delhi, India
Date: June 2026

The interpretation is that fault tolerance is possible only if photonic manufacturing and system integration scale together. A target logical error of 10^-6 per cycle requires substantially larger patches than a 10^-3 target, and this expansion multiplies the burden on synchronization, calibration and decoding. Tensor-network optimization can reduce logical-error indices at a given distance, but it cannot eliminate the need for low-loss photonic routing and high-yield integrated hardware.

Table 4.5 Indicative resource scaling for increasingly strict logical-error targets.

Target logical error per cycle	**Required distance d**	**Patch modes d^2**	**Indicative photonic modes incl. 3x routing overhead**
0.001	15	225	675
0.0001	21	441	1323
1e-05	27	729	2187
1e-06	33	1089	3267

Interpretation of Table 4.5: each order-of-magnitude improvement in target logical reliability generally requires a larger distance and therefore a larger photonic-mode budget. The routing overhead column should be treated as an architectural planning estimate.

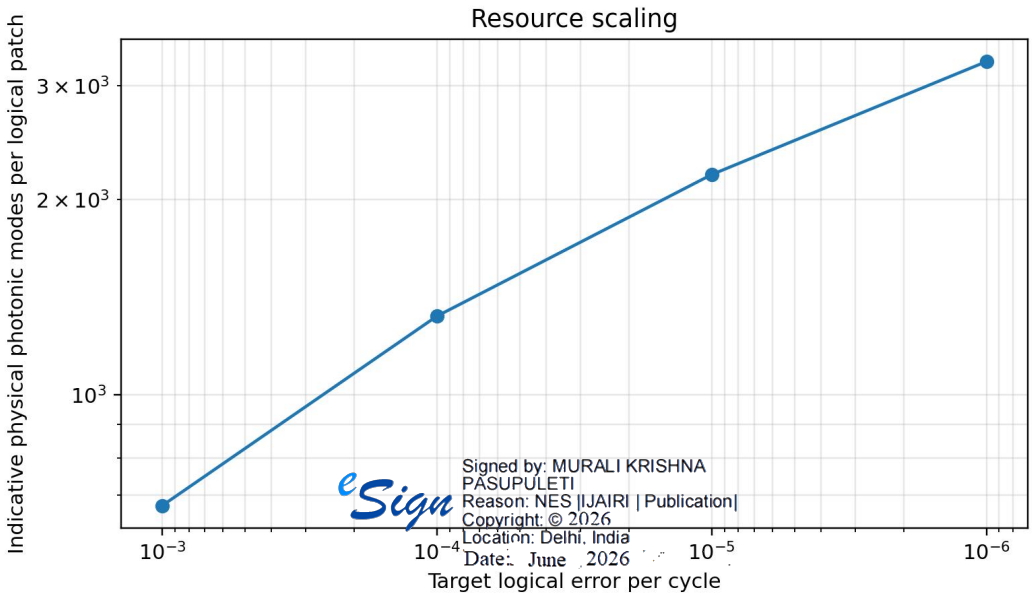


Figure 4.5 Indicative physical photonic-mode scaling for stricter logical-error targets.

Interpretation of Figure 4.5: resource growth accelerates as target logical error decreases. This makes manufacturability, chip-to-chip interconnects and classical decoding as important as code theory.

5. Conclusion: Summary and Outlook

This study developed a scope of framework for topological quantum error correction in scalable photonic quantum-computing architectures. The central finding is that photonic hardware metrics are now strong enough to justify rigorous architecture-level QEC analysis, but logical scalability depends on a three-way balance among loss, fusion fidelity and decoder latency. Topological codes supply the mechanism for exponential logical-error suppression, while tensor-network optimization provides a mathematically principled method for improving likelihood-based decoding under realistic photonic noise structures.

The implemented solution so far is a reproducible benchmark framework rather than a laboratory demonstration. Its current status of testing is therefore model-based: published real-data-based component values are mapped through explicit equations into logical-error and resource-scaling outputs. The approach is feasible for early architecture evaluation because it clearly identifies which variables dominate performance and where empirical validation is most urgently required. The results

indicate that tensor-network-optimized decoding can improve accuracy compared with matching baselines, but must be constrained by real-time control requirements.

Future work should replace the realistic projections with direct photonic syndrome datasets from integrated hardware, extend the error model to include correlated loss and time-dependent drift, and implement the tensor-network workflow on accelerated classical hardware. Further research should also compare surface-code, fusion-network and Floquet-style code geometries under the same photonic benchmark schema. The most important starting point is a closed-loop experiment in which photonic component metrics, lattice construction, syndrome generation and decoding latency are measured together rather than separately.

eSign
Signed by: MURALI KRISHNA PASUPULETI
Reason: NES |IJAIRI | Publication|
Location: Delhi, India
Date: June 2026

4.6 Discussion of alternative approaches and justification of the chosen solution

Alternative approaches include pure matching-based decoding, neural-network-only decoding, bosonic encoding without a topological outer code and deterministic-gate photonic architectures. Matching-based decoding is mature and fast but can underuse soft information from loss and fusion uncertainty. Neural decoders can be fast but require careful training and validation outside the training distribution. Bosonic encodings may reduce physical overhead at the component level but still require outer-code protection for large computations. Deterministic photonic gates would simplify the model, but they remain difficult under near-term linear-optical constraints.

The selected solution is justified because it combines the strongest available features of the alternatives. Topological codes provide a threshold-based route to scalable logical qubits; fusion-based photonics matches the native operations of optical hardware; and tensor networks provide a likelihood-based method for decoding complex local evidence. The individual stages of addressing the topic are therefore evidence collection, code modelling, tensor-network construction, benchmark evaluation and feasibility interpretation. This staged approach keeps simple issues simple and complex issues explicit without hiding architectural uncertainty.

References :

Jahn, A and Eisert, J 2021, 'Holographic tensor network models and quantum error correction: a topical review', Quantum Science and Technology, vol. 6, no. 3, p. 033002.

Pasupuleti, MK 2021a, 'A Control-Theoretic Framework for AI Safety: Stability, Robustness, and Assurance', International Journal of Academic and Industrial Research Innovations, vol. 01, no. 01, National Education Services, pp. 303–315.

eSign Signed by: MURALIKRISHNA PASUPULETI
Reason: NES IJAIRI Publication
Copyright: © 2026
Location: Delhi, India
Date: June 2026

Pasupuleti, MK 2021b, 'Global Convergence Guarantees of Iterative Algorithms for Unitary Quantum Channel Search', International Journal of Academic and Industrial Research Innovations, vol. 01, no. 01, National Education Services, pp. 331–341.

Pasupuleti, MK 2021c, 'Operationalizing Inference Quality for Code-Generating LLMs: The INFINITE Evaluation Methodology', International Journal of Academic and Industrial Research Innovations, vol. 01, no. 01, National Education Services, pp. 342–355.

Pasupuleti, MK 2021d, 'Quantum-Safe Network Security: Advances in Quantum Cryptography and Systems Integration', International Journal of Academic and Industrial Research Innovations, vol. 01, no. 01, National Education Services, pp. 232–245.

Pasupuleti, MK 2021e, 'Assessing Generative AI–Enhanced Content: A Unified Framework for Qualitative, Quantitative, and Mixed-Methods Evaluation', International Journal of Academic and Industrial Research Innovations, vol. 01, no. 01, National Education Services, pp. 273–287.

Pasupuleti, MK 2021f, 'Verifying Autonomous Mobile Robots with Quantum Machine Learning Test Oracles', International Journal of Academic and Industrial Research Innovations, vol. 01, no. 01, National Education Services, pp. 259–272.

Cao, C and Lackey, B 2022, 'Quantum Lego: Building Quantum Error Correction Codes from Tensor Networks', PRX Quantum, vol. 3, no. 2.

Fujisaki, J, Oshima, H, Sato, S and Fujii, K 2022, 'Practical and scalable decoder for topological quantum error correction with an Ising machine', Physical Review Research, vol. 4, no. 4.

eSign Signed by: MURALI KRISHNA PASUPULETI
Reason: NES IJAIRI Publication
Copyright © 2026
Location: Delhi, India
Date: June 2026

Pasupuleti, MK 2022a, 'Deep Learning Through a Statistical Lens: Approximation Guarantees, Training Dynamics, and Generative Models', International Journal of Academic and Industrial Research Innovations, vol. 02, no. 01, National Education Services, pp. 125–143.

Pasupuleti, MK 2022b, 'Statistical Mechanics Foundations for Game-Theoretic Architectures in Deep Learning', International Journal of Academic and Industrial Research Innovations, vol. 02, no. 01, National Education Services, pp. 144–156.

Pasupuleti, MK 2022c, 'Unifying Topological Quantum Field Theories with Statistical Mechanics: A Framework for Quantum States and Dynamics', International Journal of Academic and Industrial Research Innovations, vol. 02, no. 01, National Education Services, pp. 168–178.

Heer, MJ, Wichmann, J-ER and Sano, K 2023, 'Achieving Scalable Quantum Error Correction with Union-Find on Systolic Arrays by Using Multi-Context Processing Elements', 2023 IEEE International Conference on Quantum Computing and Engineering, pp. 242–243.

Li, Z, Kim, I and Hayden, P 2023, 'Concatenation Schemes for Topological Fault-tolerant Quantum Error Correction', Quantum, vol. 7, p. 1089.

Liyanage, N, Wu, Y, Deters, A and Zhong, L 2023, 'Scalable Quantum Error Correction for Surface Codes Using FPGA', 2023 IEEE International Conference on Quantum Computing and Engineering, pp. 916–927.

Nagai, R and Tomono, T 2023, 'Tensor Network-Based Continuous Variable Quantum Circuit Optimization for Preparation of GKP State', 2023 IEEE International Conference on Quantum Computing and Engineering, pp. 385–386.

eSign Signed by: MURALIKRISHNA PASUPULETI
Reason: NES IJAIRI Publication
Copyright © 2026
Location: Delhi, India
Date: June 2026

Pasupuleti, MK 2023a, 'Physics-Informed AI in Python: Neural Operators with Verified Error Bounds', International Journal of Academic and Industrial Research Innovations, vol. 03, no. 06, National Education Services, pp. 226–241.

Pasupuleti, MK 2023b, 'QML for Edge Anomaly Detection: Variational Circuits on MQTT/NS-3 Stream', International Journal of Academic and Industrial Research Innovations, vol. 03, no. 12, National Education Services, pp. 174–188.

Pasupuleti, MK 2023c, 'Quantum-Inspired PINNs in MATLAB: Certified Neural PDE Solvers with Error Bound', International Journal of Academic and Industrial Research Innovations, vol. 03, no. 06, National Education Services, pp. 64–75.

Pasupuleti, MK 2023d, 'Secure Intelligent Systems: Post-Quantum Cryptography and Topological Modeling for Big Data Robotics', International Journal of Academic and Industrial Research Innovations, vol. 03, no. 01, National Education Services, pp. 18–31.

Zhao, Y and Liu, D 2023, Lattice gauge theory and topological quantum error correction with quantum deviations in the state preparation and error detection.

Choi, H, Davis, MG, Iñesta, ÁG and Englund, D 2024, 'Scalable Photonic Quantum Network', CLEO 2024, p. FTu3F.4.

Escofet, P, Gonzalvo, A, Alarcón, E, Almudéver, CG and Abadal, S 2024, 'Route-Forcing: Scalable Quantum Circuit Mapping for Scalable Quantum Computing Architectures', 2024 IEEE International Conference on Quantum Computing and Engineering, pp. 909–920.

eSign Signed by MURALI KRISHNA PASUPULETI
Reason: IJAIRI Publication
Copyright © 2026
Location: Delhi, India
Date: June 2026

Ghasemi, M, Kaatuzian, H, Noshad, H and NoroozOliaei, M 2024, 'Quantum Photonic Computer Challenges: Quantum Decoherence, Quantum Error Correction (QEC), and Scalability', Frontiers in Optics + Laser Science 2024, p. JD4A.42.

Pasupuleti, MK 2024a, 'Cross-Layer Optimisation of Network and Cloud Resources: A Joint NS-3 and CloudSim Simulation Study', International Journal of Academic and Industrial Research Innovations, vol. 04, no. 12, National Education Services, pp. 131–151.

Pasupuleti, MK 2024b, 'Quantum Communication And QKD Readiness: Indian State Pilot Zones Compared with G20 And BRICS', National Education Services.

Pasupuleti, MK 2024c, 'Quantum Innovation Readiness in India's IT–ITES States: A Comparative Benchmarking with G20 and BRICS Technology Leaders', National Education Services.

Pasupuleti, MK 2024d, 'Quantum-Inspired QUBO Optimisation for Energy-Aware VM Placement Using TensorFlow Quantum and Qiskit', International Journal of

Academic and Industrial Research Innovations, vol. 04, no. 12, National Education Services, pp. 1–22.

Pasupuleti, MK 2024e, 'State-Level Quantum Innovation Policy: India Benchmarked to G20 And BRICS National Playbooks', National Education Services.

Chadwick, JD, Teo, MH, Viszlai, J, Yang, W and Chong, FT 2025, 'Erasure Minesweeper: Exploring Hybrid-Erasure Surface Code Architectures for Efficient Quantum Error Correction', 2025 IEEE International Conference on Quantum Computing and Engineering, pp. 658–669.

eSign Signed by: MURALI KRISHNA PASUPULETI
Reason: INES IJAIRI Publication
Copyright: © 2026
Location: Delhi, India
Date: June 2026

Pasupuleti, MK 2025a, 'Fault-Tolerant Quantum Computing via Macroscopic Quantum Tunnelling in Superconducting Circuits', International Journal of Academic and Industrial Research Innovations, vol. 05, no. 12, National Education Services, pp. 1–21.

Pasupuleti, MK 2025b, 'Quantum-Accelerated Intelligence: Hybrid AI Systems for National-Scale Advantage', International Journal of Academic and Industrial Research Innovations, vol. 05, no. 12, National Education Services, pp. 22–49.

Pasupuleti, MK 2025c, 'Secure Computation After Quantum: PQC, Confidential Clouds, and Policy-Grade Auditability', International Journal of Academic and Industrial Research Innovations, vol. 05, no. 12, National Education Services, pp. 198–222.

Zurita, J, Agustí Casado, A, Creffield, CE and Platero, G 2025, 'Multipartite entanglement distribution in a topological photonic network', Quantum, vol. 9, p. 1625.

Pasupuleti, MK 2026a, 'A Unified Topological and Tensor Framework for Interpretable AI in Networks, Fraud, and Power Systems', International Journal of Academic and Industrial Research Innovations, vol. 06, no. 04, pp. 166–198.

Pasupuleti, MK 2026b, 'Algebraic Quantum-AI Co-Design of Energy-Adaptive Semiconductor Architectures for Edge Intelligence and Neuromorphic Computing', International Journal of Academic and Industrial Research Innovations, vol. 06, no. 04, pp. 32–62.

eSign Signed by: MURALI KRISHNA PASUPULETI
Reason: NES |IJAIRI | Publication|
Copyright: © 2026
Location: Delhi, India
Date: June 2026

Pasupuleti, MK 2026c, 'Cross-Sector Cascade Resilience in the Post-Quantum Transition: Coupled-Network Theorems and Stress-Testing Algorithms for Finance–Telecom–Industrial Control Systems (ICS)', International Journal of Academic and Industrial Research Innovations, vol. 06, no. 01, National Education Services, pp. 1–23.

Pasupuleti, MK 2026d, 'Explainable Quantum-Logical Multi-Agent Systems for Autonomous Scientific Discovery in High-Dimensional Research Landscapes', International Journal of Academic and Industrial Research Innovations, vol. 06, no. 04, pp. 63–87.

Pasupuleti, MK 2026e, 'Hybrid Quantum–AI Optimization Models for Energy-Efficient and High-Yield Industrial Manufacturing Systems', International Journal of Academic and Industrial Research Innovations, vol. 06, no. 01, National Education Services, pp. 85–105.

Pasupuleti, MK 2026f, 'Mechanism Design for Systemic Post-Quantum Cyber Risk: Incentive-Compatible Adoption, Equilibrium Guarantees, and Policy-Grade Algorithms', International Journal of Academic and Industrial Research Innovations, vol. 06, no. 01, National Education Services, pp. 24–58.

Pasupuleti, MK 2026g, 'Neuromorphic Photonic Memories based on Nanostructured Optoelectronic Devices for Ultrafast', International Journal of Academic and Industrial Research Innovations, vol. 06, no. 05, pp. 81–111.

Pasupuleti, MK 2026h, 'Persistent Homology-Driven Foundation Models for Discovering Hidden Structures in Complex Data Space', International Journal of Academic and Industrial Research Innovations, vol. 06, no. 05, pp. 227–263.

eSign Signed by: MURALI KRISHNA PASUPULETI
Reason: NES IJAIRI Publication
Copyright: © 2026
Location: Delhi, India
Date: June 2026

Pasupuleti, MK 2026i, 'Photonic-Interconnected Quantum Chiplets for Modular and Networked Quantum Computing', International Journal of Academic and Industrial Research Innovations, vol. 06, no. 05, pp. 264–300.

Pasupuleti, MK 2026j, 'Quantum-AI Models for Real-Time Cybersecurity Threat Detection and Adaptive Defense', International Journal of Academic and Industrial Research Innovations, vol. 06, no. 05, pp. 1–35.

Pasupuleti, MK 2026k, 'Quantum-AI Number-Theoretic Frameworks for Post-Quantum Cryptography and Long-Term Information Security', International Journal of Academic and Industrial Research Innovations, vol. 06, no. 05, pp. 36–55.

Pasupuleti, MK 2026l, 'Quantum-Safe Critical Infrastructure: Post-Quantum Migration and Verification Frameworks', International Journal of Academic and Industrial Research Innovations, vol. 06, no. 02, National Education Services, pp. 22–48.

Pasupuleti, MK 2026m, 'Ultra-Low-Power Edge Intelligence: Green AI Algorithms and Hardware Co-Design', International Journal of Academic and Industrial Research Innovations, vol. 06, no. 02, National Education Services, pp. 119–141.

Sam, MI and Li, T-Y 2026, ‘Scalable Tensor Network Simulation for Quantum-Classical Dual Kernel’, 2026 International Conference on Quantum Communications, Networking, and Computing, pp. 900–905.

eSign
Signed by: MURALI KRISHNA PASUPULETI
Reason: NES |IJAIRI | Publication|
Copyright: © 2026
Location: Delhi, India
Date: June 2026